Remarks

Reconsideration of this application as amended is respectfully requested.

Claims 17-20 stand rejected under 35 U.S.C. § 102(e) as being unpatentable over U.S. Patent No. 5,802,113 of *Kim* ("*Kim*").

Claims 17-18 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 5,337,332 of *Yaguchi et al.* ("*Yaguchi*").

Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kim* in view of U.S. Patent No. 5,671,253 of *Stewart*.

The Examiner has rejected claims 17-20 under 35 U.S.C. § 102(e) as being anticipated by *Kim*. Applicants respectfully submit, however, that amended claim 17 is not anticipated by *Kim*. Amended claim 17 is a demodulator that includes the limitations

> a power approximation circuit coupled to receive a real and an imaginary component of a complex signal, the power approximation circuit generating an approximate power value which indicates an actual power value for the complex signal by combining absolute values of the real and imaginary components and then applying an expectation function to the combined absolute values.

(Amended claim 17, emphasis added).

Kim does not disclose a power approximation circuit as claimed in amended claim 17. Instead, *Kim* discloses a clock recovery system 30. (*Kim* col. 4, lines 47-52).

Furthermore, the clock recovery system 30 of *Kim* does not apply an expectation function to combined absolute values of signal components as claimed in amended claim 17. Instead, the clock recovery system 30 of *Kim* applies a filter function that emphasizes the recovered clock signal and excludes harmonic components. (*Kim* col. 5, lines 35-43).

In contrast to an expectation function as claimed in

amended claim 17, Fig. 4 of *Kim* shows the emphasized amplitude of the recovered clock signal in relation to the imaginary component of the signal from which it is derived.

Given that claims 18-21 depend from amended claim 17, it is submitted that claims 18-21 are not anticipated by *Kim*.

The Examiner has rejected claims 17-18 under 35 U.S.C. § 102(b) as being anticipated by *Yaguchi*. Applicants respectfully submit, however, that amended claim 17 is not anticipated by *Yaguchi*. *Yaguchi* does not disclose a power approximation circuit that applies an expectation function to combined absolute values of signal components and as claimed in amended claim 17. Instead, *Yaguchi* discloses power calculators 15 that calculate a square of the absolute value of a complex signal. (*Yaguchi* col. 6, lines 46-48). The hardware elements that compute the squares of signal components as taught by *Yaguchi* is the very type of expensive hardware that the present invention seeks to eliminate. (See page 2, lines 6-16 of the Specification).

Given that claims 18-21 depend from amended claim 17, it is submitted that claims 18-21 are not anticipated by *Yaguchi*.

Applicants further submit that claim 21 is not obvious in view of *Kim* and *Stewart*. As shown above, amended claim 17 from which claim 21 depends is not anticipated by *Kim* because *Kim* does not disclose, or suggest, a power approximation circuit that applies an expectation function to combined absolute values of signal components as claimed in amended claim 17. Moreover, *Stewart* does not disclose or suggest a power approximation circuit that applies an expectation function to combined absolute values of signal components as claimed in amended claim 17.

It is respectfully submitted that in view of the amendments and arguments set forth above, the applicable objections and rejections have been overcome.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-1078 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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Version with Markings to Show Changes Made

17. A demodulator having a power approximation circuit coupled to receive a real and an imaginary component of a complex signal, the power approximation circuit generating an approximate power value which indicates an actual power value for the complex signal by combining absolute values of the real and imaginary components [using an averaging filter] and then applying an expectation function to the combined absolute values.